

Application No.: 10/006,860
Amendment Dated: June 29, 2004
Reply to Office Action of: April 13, 2004

MTS-3296US

Remarks/Arguments:

Claims 1-6 are pending in the application.

Allowable Subject Matter:

Claim 1 is allowed.

Section 103 Rejections:

Claim 4 has been rejected as being obvious in view of Graef, Yu and Brauch. Claims 2, 3, 5 and 6 have been rejected as being obvious in view of Graef, Yu, Brauch and further in view of Bastiani and applicants' admitted prior art (APA). Applicants respectfully submit that these rejections are overcome for the reasons set forth below.

Applicants invention, is recited in amended claim 4 includes features which are not anticipated or suggested by the cited references, namely:

- an asynchronous reading and writing step of reading a predetermined amount of data from and writing the predetermined amount of data into a memory on a first-in-first-out basis, **the predetermined amount of data including a plurality of words stored in a respective plurality of address locations of the memory;**
- an error write count step of counting up by 1 **for each word of the plurality of words containing an error flag that is written into the respective plurality of address locations;**
- an error read count step of counting up by 1 **for each word of the plurality of words containing an error flag that is read from the respective plurality of address locations;**
- . . . , wherein the logic level of 1 indicates at least one error flag is set in **the plurality of words stored in the respective plurality of address locations.**

Features for amended claim 4 may be seen, for example, in allowed claim 1. Allowed claim 1 includes the features of a plurality of words stored in a respective plurality of address locations of the memory, where each word of the plurality of words contains an error flag that is written into the respective plurality of address locations. Similarly, there is an error flag for each word read from the respective plurality of address locations. After comparing values of a counter, an output of a logic level of one is provided, where the logic level of one indicates at least one error flag is set in the plurality of words stored in the respective plurality of address locations.

Application No.: 10/006,860
Amendment Dated: June 29, 2004
Reply to Office Action of: April 13, 2004

MTS-3296US

As discussed in the Response to the previous Office Action, the references of Graef, Yu, Brauch, Bastiani and Applicants' APA do not disclose the features of claim 1.

The Examiner agrees at page 9 of the Office Action that Graef, Yu, Brauch, Bastiani and Applicants' APA fail to teach each word of a plurality of words stored in a respective plurality of address locations, wherein each word of the plurality of words may contain an error flag.

Although not the same, amended claim 4 now includes features that are similar to allowed claim 1. Favorable reconsideration is respectfully requested.

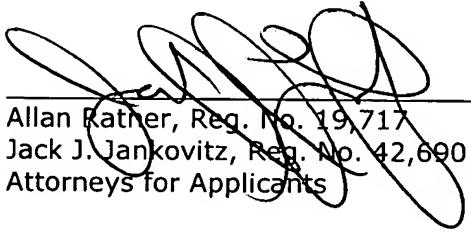
Although not the same, amended claims 2 and 5 include features similar to allowed claim 1 or amended claim 4. Favorable reconsideration is requested for amended claims 2 and 5.

Claims 3 and 6 depend from independent claims 1, 2, 4, and 5, respectively. These claims are, therefore, not subject to rejection in view of the cited references for at least the same reasons set forth for amended claim 4.

Conclusion

Claims 1-6 are in condition for allowance.

Respectfully submitted,


Allan Rather, Reg. No. 19,717
Jack J. Jankovitz, Reg. No. 42,690
Attorneys for Applicants

JJJ/ds/mc

Dated: June 29, 2004

P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

6/29/04
